

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**APPLICATION FOR LETTERS PATENT**

\* \* \* \* \*

**Semiconductor Processing Methods Of Forming A  
Conductive Gate And Line**

\* \* \* \* \*

**INVENTOR**

**Pai-Hung Pan**

ATTORNEY'S DOCKET NO. MI22-488

**EL054827 024**

EM 10/10/2000

1 TECHNICAL FIELD

2 (a) This invention relates to semiconductor processing methods of  
3 forming a conductive gate line.

5 BACKGROUND OF THE INVENTION

6 Metal Oxide Semiconductor (MOS) devices find use in integrated  
7 circuit memory devices such as static random access memory (SRAM)  
8 and dynamic random access memory (DRAM) devices. Such devices  
9 inevitably include conductive lines connecting one or more of the devices  
10 together. One type of conductive line is a gate or word line. Word  
11 lines connect the gates of one or more MOS devices together so that  
12 when the word line is turned on, data in the form of stored charges  
13 can be accessed.

14 It is desirable that a word line be highly conductive. A great  
15 deal of effort has gone into engineering more conductive word lines.  
16 Word lines are typically formed over a dielectric surface. The  
17 conventional word line includes at least one layer of conductive material  
18 which is layered onto the dielectric surface and then etched, typically  
19 anisotropically, to form a patterned word line, also referred to herein  
20 as a gate, gate line or gate stack. After anisotropically etching the  
21 gate or gate line, it is desirable to conduct a reoxidation step which  
22 helps to repair damage to the dielectric surface resulting from the  
23 anisotropic etch. Additionally, the reoxidation step oxidizes a portion  
24 of the gate or gate stack immediately adjacent the dielectric surface to

round the lower portion of the conductive material, effectively creating a so-called "smiling gate" structure in which tiny bird's beak structures are formed at the bottom corners of the gate stack. Such smiling gate structure reduces hot electron degradation, as recognized by those of skill in the art.

During such reoxidation steps, it has been observed that the conductivity of the gate has been impaired due to the undesirable oxidation of the conductive materials forming the gate. For example, one type of conductive gate includes a conductive polysilicon layer atop the dielectric surface and a conductive layer of  $WSi_x$  atop the polysilicon layer. A more conductive prior art word line is formed from a conductive layer of polysilicon, a conductive layer of metallic material, and an intervening conductive metallic barrier layer between the polysilicon and metallic material which prevents formation of silicide during subsequent processing. Unfortunately, during the reoxidation step, the conductive materials of the line experience appreciable oxidation which has led to higher resistances (lower conductivities). Additionally, such oxidation has led to degradation of the interface between the materials which, in turn, can cause the materials to peel away from one another and create a yield loss.

This invention grew out of the need to provide a conductive line and to reduce undesirable oxidation effects on the conductive line due to oxidation processing steps such as a source/drain oxidation.

1      **BRIEF DESCRIPTION OF THE DRAWINGS**

2      Preferred embodiments of the invention are described below with  
3      reference to the following accompanying drawings.

4      Fig. 1 is a diagrammatic representation of a fragment of a  
5      substrate processed in accordance with the invention.

6      Fig. 2 is a view of the Fig. 1 substrate fragment at a processing  
7      step subsequent to that shown by Fig. 1.

8      Fig. 3 is a view of the Fig. 1 substrate fragment at a processing  
9      step subsequent to that shown by Fig. 2.

10     Fig. 4 is a view of the Fig. 1 substrate fragment at a processing  
11    step subsequent to that shown by Fig. 3.

12     Fig. 5 is a view of the Fig. 1 substrate fragment at a processing  
13    step subsequent to that shown by Fig. 4.

14     Fig. 6 is a view of the Fig. 1 substrate fragment at a processing  
15    step subsequent to that shown by Fig. 2 in accordance with an alternate  
16    preferred embodiment of the invention.

17     Fig. 7 is a view of the Fig. 1 substrate fragment at a processing  
18    step subsequent to that shown by Fig. 6.

19     Fig. 8 is an enlarged view of a portion of the wafer fragment of  
20    Fig. 3 undergoing a smiling gate oxidation.

1      **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

2      This disclosure of the invention is submitted in furtherance of the  
3      constitutional purposes of the U.S. Patent Laws "to promote the  
4      progress of science and useful arts" (Article 1, Section 8).

5      In accordance with one aspect of the invention, a semiconductor  
6      processing method of forming a conductive transistor gate over a  
7      substrate comprises the steps of:

8      forming a conductive gate over a gate dielectric layer on a  
9      substrate, the gate having sidewalls and an interface with the gate  
10     dielectric layer;

11     forming nitride containing spacers over the gate sidewalls; and

12     after forming the spacers, exposing the substrate to oxidizing  
13     conditions effective to oxidize at least a portion of the gate interface  
14     with the gate dielectric layer.

15     In accordance with another aspect of the invention, a  
16     semiconductor processing method of forming a conductive gate comprises  
17     the steps of:

18     forming a patterned gate atop a substrate dielectric surface, at  
19     least a portion of the gate being conductive;

20     covering the gate with oxidation resistant material; and

21     exposing the substrate to oxidation conditions effective to oxidize  
22     at least a portion of the gate laterally adjacent the oxidation barriers

1                   In accordance with yet another aspect of the invention, a  
2 semiconductor processing method of forming a conductive transistor gate  
3 over a substrate comprises the steps of:

4                   forming a conductive gate over a gate dielectric layer on a  
5 substrate, the gate having sidewalls;

6                   forming non-oxide spacers over the sidewalls; and

7                   after forming the spacers, exposing the substrate to oxidizing  
8 conditions effective to oxidize at least a portion of the gate and a  
9 portion of the substrate beneath the gate.

10                  More specifically and with reference to Fig. 1, a semiconductor  
11 wafer fragment in process is indicated generally by reference  
12 numeral 10. Such is comprised of a bulk substrate 12, preferably  
13 composed of monocrystalline silicon, and an overlying dielectric layer 14  
14 in the form of a suitable gate oxide. Dielectric layer 14 defines a  
15 substrate dielectric surface atop which a patterned composite gate or  
16 gate stack 16 is formed, preferably by an anisotropic reactive ion etch.  
17 Gate stack 16 defines a field effect transistor gate line at least a  
18 portion of which is conductive. Gate stack 16 includes a pair of  
19 sidewalls 18, 20 and an interface 22 with gate dielectric layer 14. Gate  
20 stack 16 is a multi-layered structural composite which includes a  
21 plurality of layers. A first conductive layer 24 is preferably formed  
22 from polysilicon and includes a portion which defines interface 22. A  
23 metal layer 26 overlies layer 24 and is formed from a suitable metal  
24 such as tungsten (W), molybdenum (Mo) and the like. An electrically

1 conductive reaction barrier layer 28 is preferably formed from a suitable  
2 material such as TiN, WN, and the like and is interposed between or  
3 intermediate layers 24 and 26. Layer 28 in the preferred embodiment  
4 prevents the formation of a silicide during subsequent processing steps.  
5 A cap 30 is formed atop overlying metal layer 26 from a suitable  
6 oxidation resistant material such as oxide/nitride, nitride,  
7 oxide/nitride/oxide, oxynitride, Si-rich nitride and the like, for protecting  
8 or shielding gate stack 16 during a subsequent oxidation step described  
9 in detail below. Accordingly, cap 30 is a nitride containing material  
10 which effectively protects or shields the top of the gate line as will  
11 become apparent below.

12 Referring to Figs. 2 and 3, first oxidation barriers are formed on  
13 gate stack 16 which cover at least the conductive portion of the gate  
14 stack. First oxidation barriers can be formed from nitride containing  
15 material and/or suitable non-oxide materials. More specifically, first  
16 oxidation barrier material 32, such as  $Si_3N_4$  or  $SiN_xO_y$ , is deposited  
17 over gate stack 16 (Fig. 2) to a thickness ranging from between 50 to  
18 500 Angstroms. Such can be deposited utilizing conventional techniques  
19 at deposition temperatures between 300°C - 900°C. A subsequent first  
20 anisotropic etch (Fig. 3) is conducted to a degree sufficient to leave  
21 first oxidation barriers 34, 36 on or proximate gate stack 16.  
22 Preferably, such etch is a reactive ion etch which is selective to oxide.  
23 Oxidation barriers 34, 36 preferably shield at least a portion of gate  
24 line sidewalls 18, 20 during subsequent processing, which includes a

1 reoxidation step described below. For purposes of the ongoing  
2 discussion, first oxidation barrier material 32 comprises a first insulative  
3 or insulating material which is anisotropically etched to form electrically  
4 insulative or insulating spacers 34, 36 over gate line sidewalls 18, 20,  
5 respectively.

6 According to one preferred aspect of the invention, and after  
7 spacers or barriers 34, 36 are formed, the substrate is exposed to  
8 oxidizing conditions which are effective to reoxidize the substrate to  
9 repair damage to layer 14 resulting from the first etch, as well as to  
10 oxidize at least a portion of the gate or gate line interface 22 with  
11 dielectric layer 14. During such exposure cap 30 together with barriers  
12 34, 36 effectively encapsulate or cover the gate thereby preferably  
13 shielding the gate top and desired portions of the gate sidewalls from  
14 the effects of oxidation. Suitable oxidizing conditions have been found  
15 to be those which are conducted at ambient temperatures in a range  
16 from between about 800°C to 1050°C for time periods which would be  
17 sufficient to grow an oxide layer over a separate semiconductor  
18 substrate to a thickness of around 80 Angstroms. Other oxidizing  
19 conditions are possible. Such oxidation is best seen in Fig. 8 which is  
20 an enlarged partial view of gate or gate stack 16. There, bottom  
21 corner portions of polysilicon layer 24 laterally adjacent spacers 34, 36  
22 are suitably oxidized and thereby rounded to form a smiling gate.  
23 More specifically, oxidants indicated by the small arrows entering into  
24 and through gate dielectric layer 14 channel along and through dielectric

layer 14. That is, layer 14 provides a channeling layer through which oxidants can travel to reach the gate or gate stack. Preferably during the smiling gate oxidation, the portion of gate stack 16 which is oxidized is disposed laterally adjacent and inwardly of barriers or spacers 34, 36 and forms a "bird's beak" structure immediately adjacent each respective spacer. By controlling the oxidation temperature and time as mentioned above, the oxidation will occur at preferred gate edge regions and will not appreciably propagate upwardly towards layers 26, 28.

The smiling gate oxidation step may, however, be conducted at processing points other than immediately following the formation of spacers 34, 36. Such is described by way of example immediately below.

Referring to Fig. 4, another preferred aspect of the invention is set forth in which the smiling gate oxidation step is conducted after a second barrier material 38 is deposited over substrate 12, and more specifically, deposited over barriers or spacers 34, 36 which are defined by first barrier material 32. Preferably, the second barrier material is a nitride containing and/or non-oxide material deposited to a thickness of 500 Angstroms. For purposes of the ongoing discussion, second barrier material 38 is a second oxidation resistant layer or an electrically insulating or insulative material.

Referring to Fig. 5, a second anisotropic etch, preferably a reactive ion etch of second barrier material 38 is conducted to a degree

sufficient to leave second oxidation barriers 40, 42 over or proximate first oxidation barriers 34, 36 respectively. At this point, the smiling gate oxidation can take place to form the smiling gate as described above with reference to Fig. 8. The step of exposing the substrate to the oxidation conditions sufficient to form the smiling gate as described above, can take place prior to depositing second barrier material 38 and after the first anisotropic etch. Such step would take place in conjunction with gate stack 16 as shown in Fig. 3.

Referring to Fig. 6, another preferred aspect of the invention is set forth in which the smiling gate oxidation step takes place after contemporaneous formation of the first and second oxidation barriers. Specifically, first and second barrier materials or layers 32, 38 are deposited over gate stack 16 as shown without anisotropic etch of layer 32 prior to provision of layer 38. Preferably, the respective thickness of such layers are 100 Angstroms (layer 32) and 500 Angstroms (layer 38).

Referring to Fig. 7, an anisotropic etch, preferably a reactive ion etch of first and second barrier materials 32, 38 is conducted to a degree sufficient to leave oxidation barriers 44, 46 on or over gate stack 16. When oxidation barriers are formed according to this aspect of the present method, the resulting barriers or spacers have a construction which is somewhat different from that shown in Fig. 5. More specifically, first or inner spacers 48, 50 include a bottom portion which abuts dielectric layer 14 and extends laterally away from gate

1 stack 16 forming an L-shape (spacer 50) or a reverse L-shape  
2 (spacer 48).

3 After gate line sidewalls 18, 20 have been suitably electrically  
4 insulated, substrate 12 is exposed to oxidizing conditions which are  
5 effective to oxidize at least a portion of gate line interface 22 as  
6 described above, thereby forming the desired smiling gate construction.  
7 The anisotropic etch which is conducted with reference to Figs. 6  
8 and 7, is a common step anisotropic etch which contemporaneously  
9 forms the desired spacers or barriers described above.

10 The preferred methods of forming the desired smiling gate  
11 structure include, first shielding the gate or gate line sidewalls or  
12 conductive portions thereof with a suitable shielding material, and then  
13 conducting a reoxidation step, such as a source/drain reoxidation step,  
14 which utilizes dielectric layer 14 as a suitable channeling layer or  
15 medium along and through which oxidants travel to reach first  
16 conductive layer 24 so as to oxidize a portion thereof and a portion  
17 of the substrate therebeneath. According to a preferred aspect the  
18 shielding step includes, in a separate step, forming cap 30 over the gate  
19 top to protect the gate top during oxidation exposure. The oxidation  
20 barriers, whether barriers 34, 36 (Fig. 3), barrier pairs 34/40, 36/42 (Fig.  
21 5), or barrier pairs 44/48, 46/50 (Fig. 7), serve to protect, along with  
22 oxidation resistant cap 30, the transistor gate or gate line stack from  
23 being undesirably affected by the reoxidation step which creates the  
24 smiling gate construction. This is because during such reoxidation step,

1 the materials utilized to form composite gate stack 16 are effectively  
2 encapsulated or covered with oxidation barriers and sealed. Such serves  
3 to protect against undesirable chemical reactions with the oxidants.  
4 Such chemical reactions, if allowed to take place, would undesirably  
5 erode or oxidize the gate stack materials.

6 In compliance with the statute, the invention has been described  
7 in language more or less specific as to structural and methodical  
8 features. It is to be understood, however, that the invention is not  
9 limited to the specific features shown and described, since the means  
10 herein disclosed comprise preferred forms of putting the invention into  
11 effect. The invention is, therefore, claimed in any of its forms or  
12 modifications within the proper scope of the appended claims  
13 appropriately interpreted in accordance with the doctrine of equivalents.

14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24